# Quiz 2

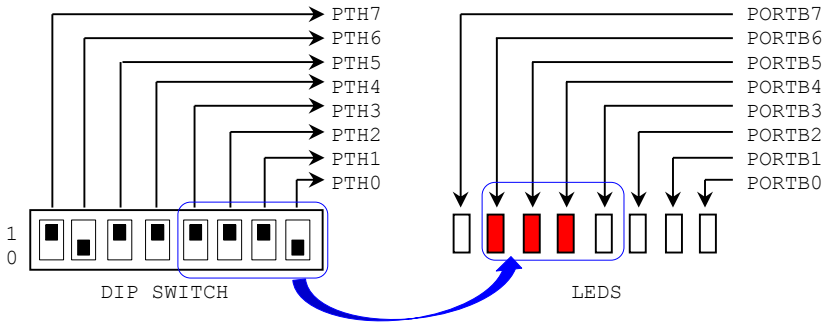
(October 14th @ 5:30 pm)

## Problem 1 (40 pts)

- Given a 25 MHz bus clock, provide a set of instructions to generate a time delay of 40 ms. Consider that `pusha` takes 2 cycles, `pula` 3 cycles, `nop` one cycle and `dbne` 3 cycles.

## Problem 2 (20 pts)

- Complete the Assembly Program below so that the state of the four rightmost bits on the DIP Switch is only displayed on the bits 6, 5, 4, and 3 of PORTB (the LEDs). The figure shows an example on the Dragon12-Light Board: the number `1110` is shown on the bits 6, 5, 4, and 3 while the other LEDs are off.




```
ROMStart    EQU  $4000

; code section
            ORG   ROMStart

Entry:
_Startup:
            LDS   #$4000

            movb #$FF, DDRB
            movb #$00, DDRH


showDIPSW:  ldaa PTH

            /* Write instructions here */
```

```
            /* End of your instructions */
            staa PORTB     ; Contents of register A are written on PORTB
            bra showDIPSW
```

# PROBLEM 3 (40 PTS)

- Given the following Assembly code, specify the `SP` and the Stack Contents at the given times (right after the colored instruction has been executed). `SP` and the Stack Contents (empty) are specified for the first instruction (`LDS #$4000`).
- Specify a value in the instruction `addb` that would make the branch instruction `bcs` branch to `mloop`.